Claims

We claim:

1. A digital-to-analog converter (DAC) coupled to receive at least one digital input signal and a clock signal, comprising:

a current cell driving circuit for generating first and second synchronous control signals, wherein the current cell driving circuit includes

a decoder to decode the digital input signal into a first and second code sequence signal, and

a latch for latching the first and second code sequence signal depending upon the clock signal and for providing the first and second synchronous control signal, wherein the latch includes a plurality of transistors; and

a current cell, having a plurality of output current source transistors, to operate as a current source depending upon the first and second synchronous control signals;

wherein the latch reduces the drain to source voltage variation of the plurality of output current source transistors and reduces the coupling of unwanted injection of the digital input signal and the clock signal by maintaining the plurality of transistors of the latch in the off position during code transitions without compromising the DAC update speed.

2. A digital-to-analog converter (DAC) as recited in claim 1, wherein the latch comprises:

a first subcircuit portion having a first input node and first output node, wherein the first input node coupled to receive the first differential signal to enable the first differential signal to be transmitted when the clocking signal is high;

a second subcircuit portion having a second input node and second output node wherein the second input node coupled to receive the second

differential signal to enable the second differential signal to be transmitted when the clocking signal is high;

a first PMOS transistor, having a gate, a drain and a source, the source coupled to the power supply, the gate coupled to receive the clocking signal;

a second PMOS transistor, having a gate, a drain and a source, the source coupled to the drain of the first PMOS transistor, the gate coupled to the first output node of the first subcircuit portion;

a third PMOS transistor, having a gate, a drain and a source, the source coupled to the drain of the first PMOS transistor, the gate coupled to the second output node of the second subcircuit portion;

a first inverter, having an input and output, the first inverter coupled between the drain of the second PMOS transistor and the drain of the third PMOS transistor;

a second inverter, having an input and output, the second inverter coupled in parallel with the first inverter, wherein the input of the first inverter coupled to the output of the second inverter and the output of the first inverter coupled to the input of the second inverter;

a third inverter coupled to the drain of the second PMOS transistor; and

a fourth inverter coupled to the drain of the third PMOS transistor.

3. A apparatus as recited in claim 2, wherein the first subcircuit portion comprises:

a first NMOS transistor having a gate, a source, and a drain, the gate coupled to receive the inverted clock signal,

a fourth PMOS transistor having a gate, a source, and a drain, the gate coupled to receive the clock signal, the drain coupled to the drain of the first NMOS transistor to form a first output node, the source coupled to the source of the first NMOS transistor to form a first input node, the first input node coupled to receive the first differential signal.

4. A apparatus as recited in claim 2, wherein the a second subcircuit portion comprises:

a first NMOS transistor having a gate, a source, and a drain, the gate of the NMOS transistor coupled to receive the inverted clock signal,

a fourth PMOS transistor having a gate, a source, and a drain, the gate coupled to receive the clock signal, the drain coupled to the drain of the first NMOS transistor to form a second input node, the source coupled to the source of the first NMOS transistor to form a second output node, the first input node coupled to receive the second differential signal.